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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/592,572	06/12/2000	Richard Dellacona	QUAD:55767	4159

7590 07/28/2006

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 09/592,572	**Applicant(s)** DELLACONA, RICHARD	
	Examiner Kandasamy Thangavelu	**Art Unit** 2123	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 06 July 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Attachment-A.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

7/20/06

ATTACHMENT – A: ADVISORY ACTION

1. This communication is in response to the Applicants' response dated July 6, 2006. Applicants' arguments filed on July 6, 2006 have been fully considered. Applicants' arguments, filed on July 6, 2006 under 35 U.S.C. 103 (a) are not persuasive.

Arguments

2.1 As per the Applicants' argument that "there is no teaching, disclosure or suggestion in Brant et al. that the programmable processor which is used to control the storage units S1-S5 independently of the CPU can be used to establish direct communication between the two controllers, or maintain direct communication between the two controllers independently of the CPU, or that the two controllers maintain direct communication between the two controllers independent of the CPU", the Examiner respectfully disagrees.

Brant et al. teaches at CL7, L20-28 that each controller includes a separately programmable processor which can act independently of the CPU to control storage units. **Brant et al.** shows in Fig. 4 two controllers connected to the CPU; each controller has direct communication with the other controller. **Brant et al.** teaches at CL12, L64 to CL13, L8 that each controller is identical to the controller described at CL7, L20-28. **Brant et al.** shows in Fig. 8 that each controller communicates with the other controller

using the controller processor and data link interface, independent of the CPU. **Brant et al.** states at CL13, L33-35 that if one controller fails, the other controller assumes operational control of both logical arrays, implying that there is communication between the controllers to determine the status of the other controller. **Brant et al.** teaches at CL18, L42-52 that each controller has a controller processor and a controller-to-controller interface and at CL20, L50-63 that data can be transmitted from one array controller to another array controller. The controller-to-controller interface is responsible for transmitting data to and from the other controller.

Therefore, the Examiner takes the position that the programmable processor of the controller can be used to establish direct communication between the two controllers and maintain direct communication between the two controllers independently of the CPU and that the two controllers maintain direct communication between the two controllers independent of the CPU.

2.2 As per the Applicants' argument that "there is no teaching, disclosure or suggestion that the memory interfaces, which could presumably include a processor to communicate with storage independent of the CPU, are equivalent to the controller-controller interfaces; implementing the modification suggested by the Examiner would only allow the controller-controller interfaces the ability to control the storage units independently of the CPU, but not to control and maintain direct communication between the two controllers independent of the CPU", the Examiner respectfully disagrees.

The examiner has not stated that memory interfaces are equivalent to the controller-to-controller interface.

Brant et al. teaches at CL7, L20-28 that each controller includes a separately programmable processor which can act independently of the CPU to control storage units. **Brant et al.** shows in Fig. 4 two controllers connected to the CPU; each controller has direct communication with the other controller. **Brant et al.** teaches at CL12, L64 to CL13, L8 that each controller is identical to the controller described at CL7, L20-28. **Brant et al.** shows in Fig. 8 that each controller communicates with the other controller using the controller processor and data link interface, independent of the CPU. **Brant et al.** states at CL13, L33-35 that if one controller fails, the other controller assumes operational control of both logical arrays, implying that there is communication between the controllers to determine the status of the other controller. **Brant et al.** teaches at CL18, L42-52 that each controller has a controller processor and a controller-to-controller interface and at CL20, L50-63 that data can be transmitted from one array controller to another array controller. The controller-to-controller interface is responsible for transmitting data to and from the other controller.

Therefore, the Examiner takes the position that since each controller has a controller processor and a controller-to-controller interface and data can be transmitted from one array controller to another array controller, there is no need to modify **Brant et al.** Only Leshem in view of Espy, Horst et al., Hillis, Dekoning, et al. and Swanson et al. needs to be modified by **Brant et al.**

Therefore, the Examiner takes the position that the programmable processor of the controller can be used to establish direct communication between the two controllers and

maintain direct communication between the two controllers independently of the CPU and that the two controllers maintain direct communication between the two controllers independent of the CPU.

2.3 As per the Applicants' argument that "In Fig. 4, there is no teaching, disclosure or suggestion in Brant et al. that the programmable processor which is used to control the storage units S1-S5 independently of the CPU can be used to establish direct communication between the two controllers 403, 405, or maintain direct communication between the two controllers independently of the CPU, or that the two controllers-maintain direct communication between the two controllers independent of the CPU" the Examiner respectfully disagrees. The Examiner directs Applicants' attention to Paragraph 2.1 above.

3. In view of the above explanation, the request for reconsideration has been considered but is not persuasive and does not place the application in condition for allowance.

K. Thangavelu
Art Unit 2123
July 20, 2006